Form PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. MI22-2054	SERIAL NO. 10/688828 Filed Herewith
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)		APPLICANT Paul A. Farrar	
		FILING DATE Filed Herewith 10/17/03	GROUP Unknown 2827

U.S. PATENT DOCUMENTS

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
TL	AA	5,920,785	7/6/1999	Chi et al.			
TL	AB	6,184,548 B1	2/6/2001	Chi et al.			
TL	AC	3,387,282	6/4/1968	Jaques, J.O.			
TL	AD	US 2002/0009874	1/24/2002	Farrar et al.			
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						

EL979977585

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
	AM							
	AN							
	AO							
	AP							
	AQ							

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

TL	AR		*SEMICONDUCTORS: IBM, Infineon Open Trench Warfare Over 1-Gbit Design;* Anthony Cataldo; http://www.eetimes.com/semi/news/OEG19991028S0038; October 28, 1999; 5 pps.
TL	AS		*A Novel Trench DRAM Cell with a VERtical Access Transistor and BuriEd STrap (VERY BEST) for 4GB/16Gb;* U. Gruening, C.J. Radens, J.A. Mandelman, A. Michaelis, M. Seitz, N. Arnold, D. Lea, D. Casarotto, A. Knorr, S. Halle, T.H. Ivers, L. Economikos, S. Kudelka, S. Raha, H. Tews, H. Lee, R. Divakaruni, J.J. Welser, T. Furukawa, T. S. Kanarsky, J. Alsmeier, G. B. Bronner; printed September, 1999; 4 pps.

EXAMINER	DATE CONSIDERED
Moyle	4/7/06

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.